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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/408,429	09/29/1999	MIKLOS SANDORFI	07072/086001	4042

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DALY, CROWLEY & MOFFORD, LLP
SUITE 101
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CANTON, MA 02021-2310

EXAMINER
TRAN, DENISE

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 03/12/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

NM

Office Action Summary	Application No.	Applicant(s)	
	09/408,429	SANDORFI, MIKLOS	
	Examiner	Art Unit	
	Denise Tran	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 February 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *8, 10* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1-19 are presented for examination.

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 18 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 18 contains the trademark/trade name Power PC, line 2. Where a trademark or trade name is used in a claim as a limitation to identify or describe a particular material or product, the claim does not comply with the requirements of 35 U.S.C. 112, second paragraph. See *Ex parte Simpson*, 218 USPQ 1020 (Bd. App. 1982). The claim scope is uncertain since the trademark or trade name cannot be used properly to identify any particular material or product. A trademark or trade name is used to identify a source of goods, and not the goods themselves. Thus, a trademark or trade name does not identify or describe the goods associated with the trademark or trade name. In the present case, the trademark/trade name is used to identify/describe microprocessor and, accordingly, the identification/description is indefinite.

4. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11

F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

5. Claims 1-19 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-16 and 17-18 of copending Application No. 09/408,807. Although the conflicting claims are not identical, they are not patentably distinct from each other. The claims of the current application do not have a controller for producing a control signal; however, both the concept and the advantages of providing a controller for producing a control signal are well known and expected in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to comprise a controller for producing a control signal because it would allow enhancing to the system controlling.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stolt et al., U.S. Patent No. 5721860, (hereinafter Stolt), in view of Chin et al., U.S. Patent No. 6286083 B1, (hereinafter Chin).

As per claim 1, Stolt teaches the invention substantially as claimed, a microprocessor interface disposed between a memory and a microprocessor (e.g., fig.1, el. DP or MC), comprising: a semi conductor integrated circuit (e.g., col. 3, line 32 and et seq.); a data rebuffering section (e.g., fig. 2, el. Buffers, DPU, IRQ, BED, DPU) adapted to couple data from a one of a plurality of data ports to a data port of a microprocessor selectively in accordance with a control signal (e.g. figs 1-2, BED coupling one of data ports to a microprocessor port in accordance with a read/write control signal; col. 4, lines 49 and et seq.); a main memory interface (e.g., fig. 2, el. MMID and/or MCL) adapted for coupling to the memory for the microprocessor, such main memory interface being coupled to the data rebuffering section for providing control signals to the memory for enabling data transfer between the memory and the microprocessor through the data rebuffering section (e.g., col. 5, line 22 and et seq.).

Stolt does not explicitly show a main memory. Chin shows a main memory (e.g., col. 5, line 5 and et seq.) as well known and expected in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the SDRAM/ADRAM memory of Stolt as a main memory because it would provide storing application programs and data for the system.

As per claims 2-4, 9-11, Stolt shows wherein the memory is a selected one of a plurality of memory types each (e.g., abstract) and wherein the main memory interface is configured in accordance with the selected one of the plurality of memory types to provide data being transferred between the processor and the memory through the main memory interface (e.g., col. 5, line 22 and et seq.); and one memory type is a SDRAM; each memory type having a different data transfer protocol and the main memory interface is configured to provide a proper memory protocol to data being transferred (e.g., col. 2, line 11 and et seq.; col. 5, line 35 and et seq.). Stolt does not explicitly show a main memory. Chin shows a main memory (e.g., col. 5, line 5 and et seq.) as well known and expected in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the SDRAM/ADRAM memory of Stolt as a main memory because it would provide storing application programs and data for the system. Furthermore, Stolt does not explicitly show the use of RDRAM. "Official Notice" is taken that both the concept and the advantages of providing RDRAM are well known and expected in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a RDRAM because it would provide a high speed memory accessing.

As per claim 5-8, Stolt shows a second integrated circuit for controlling the first integrated circuit (e.g., fig.2, DC component), having a controller adapted for coupling to the main memory interface, such controller being adapted to produce a main memory access control signal (e.g., fig. 2, IRQ, ORQ); the data rebufferring section including a selector responsive to the control signal for coupling data between a selected one of the data ports and the data port of the processor (e.g., fig. 2, el. BED, QMUD, DPU including transfer signals responsive to a command to select the flow of data; and col. 5, line 20 and et seq.); the data rebufferring section including a selector responsive to a control signal for coupling the data port of the processor to either :a selected one of data port; or the main memory (e.g., fig. 2, el. BED, QMUD, DPU including transfer signals responsive to a command to select the flow of data; and col. 5, line 20 and et seq.); a data distribution unit having a plurality of ports each one of the ports being coupled to a corresponding one of: a selector, a RAM, an interrupt request controller, the processor port, and the main memory interface (e.g., fig. 2, el. BED, QMUD, DPU). Stolt does not explicitly show a main memory has a two portion address locations, one portion being addressed by the main memory interface in response to the processor and the other portion being addressed by the main memory interface in response to the controller. Chin shows a main memory (e.g., col. 5, line 5 and et seq.) as well known and expected in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the SDRAM/ADRAM memory of Stolt as a main memory because it would provide storing application programs and data for the system. "Official Notice" is taken that both the concept and the advantages of providing a memory with

separate address portions for a different controller are well known and expected in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a memory with two portion address locations being addressed by two controllers because it would allow data processing independently and data integrity.

As per claims 12-14 and 19, Stolt shows the main memory interface comprising: a processor/main memory interface control section adapted to provide control signals between section and the processor and the controller (e.g., fig. 2, els. ICIC, DSPM, registers and/ or IRQ, ORQ, MCL). Stolt show each memory type having a different data transfer protocol and a main memory controller is configured to provide a proper memory protocol to data being transferred between the microprocessor and memory through the main memory interface (e.g., fig. 2, els. ICIC, DSPM, registers and/ or IRQ, ORQ, MCL; col.2, line 11 and et seq. and col. 8, line 10 and et seq.) and being configured in accordance with a control signal provided by the microprocessor to address a selected one of a plurality of potential memory capacities, the control signal supplied by the microprocessor indicating to the main memory controller the particular one of the plurality of potential memory capacities of the main memory (e.g., col.7, line 18 and et seq.). Stolt and Chin do not explicitly show a mask to transform the address to an address in the second section of the memory. "Official Notice" is taken that both the concept and the advantages of providing a mask to transform the address are well known and expected in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a mask to transform the address to

Stolt and Chin because it would provide a selected group of bits of an address, thereby it allow independently, and flexibility supporting a different types of memory addresses portions.

As per claims 15-18, Stolt teaches one memory type is a SDRAM (e.g., abstract); the main memory interface including an error correction and detection unit coupled between the distributor and the main memory controller (e.g., fig. 2, el. Error bus; col.4, line 42 and et seq.); Stolt does not explicitly show the use of RDRAM and Power PC microprocessor. "Official Notice" is taken that both the concept and the advantages of providing RDRAM are well known and expected in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a RDRAM because it would provide a high speed memory accessing. . "Official Notice" is taken that both the concept and the advantages of providing Power PC microprocessor are well known and expected in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a Power PC microprocessor because it would maintain compatibility with the other components IBM product.

8. Applicant's arguments filed 2-8-02 have been fully considered but they are not persuasive.

9. In the remarks, the applicant argued (1) that Stolt does not show or suggest Applicant's central processing unit including: (i) a data rebuffering section disposed in a

chip and adapted to couple data from a one of a plurality of data ports to a data port of the microprocessor selectively in accordance with a control signal.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., central processing unit including:) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

In further discussion, the examiner disagree with the applicant's argument that "the DP has only one data port" because according to figs.1 and 2, DP has a plurality of data ports, such as read data ports and write data ports of BED coupled to a data port of a microprocessor selectively in accordance with a read/write control signal or a request from one of a plurality requesters (e.g., col. 4, line 49 and et seq.). Also, the Examiner would like to bring to the applicant's attention that data may not be directly passed from the DC to the data ports of the microprocessors but the data port of DC in fig. 2 is still a data port. Thus, Stolt, Figs. 1-2 and e.g., col. 4, line 49 and et seq. shows a data rebuffering section (e.g., fig. 2, el. Buffers, DPU, IRQ, BED, DPU) disposed in a chip (e.g., col. 3, lines 32-36) and adapted to couple data from a one of a plurality of data ports to a data port of the microprocessor selectively in accordance with a control signal (e.g., read/write control or a request from one of a plurality requesters).

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Denise Tran whose telephone number is (703) 305-9823. The examiner can normally be reached on Monday, Thursday, and an alternate Wed. from 8:30 a.m. to 6:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (703) 305-3821. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

DT

D.T.
March 8, 2002

MATTHEW KIM
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